REMARKS

Rejections Under 35 USC §112, first paragraph

Claims 77-82 have been rejected under 35 USC §112, first paragraph, due to the limitation "spring loaded electrical connectors". In response to these rejections, the term "spring loaded" has been deleted from the claims. Antecedent basis for the term "electrical connectors" is contained on page 14, lines 18-19, in referring to pogo pins 42. In addition, the pogo pins 42 are shown in Figure 7B.

Rejections Under 35 USC §112, second paragraph

Claims 77-82 have been rejected under 35 USC §112, second paragraph, as being indefinite due to: "It not being clear what parts of the disclosed apparatus would be used in performing the claimed method". In response to these rejections, independent claim 77 has been amended to simplify, and more clearly state elements of the apparatus used to perform the method. In addition, claim 79 has been amended to remove the "pogo" recitation.

Claims 77-82 recite a test method using a testing apparatus, which as shown in Figure 7B, includes electrical connectors in the form of pogo pins 42, which are configured to transmit test signals, and to also apply a biasing force.

A reading of claim 77 on the drawings and specification is as follows.

77. A method **(page 8, lines 13-26)** for testing a semiconductor wafer **(12-Figure 1)** comprising:

providing a testing apparatus **(78-Figure 8, page 26, lines 10-27)** comprising a test circuitry **(44-Figure 8, page 26, lines 14-18)** configured to apply test signals to the wafer, a suspended plate **(80LP-Figure 7B, page 23, lines 21-34, antecedent basis for "suspended" on page 21, line**

3), a substrate **(16-Figure 7B, page 23, lines 19-22)** on the suspended plate, and a force applying mechanism **(32-Figure 1 page 12, lines 19-21)** comprising a plurality of electrical connectors **(42-Figure 7B, antecedent basis for "electrical connectors" on page 14, lines 18-19)** in contact with the suspended plate in electrical communication with the test circuitry **(page 24, line 34 to page 25, line 3)**;

biasing the substrate against the wafer using the suspended plate and the force applying mechanism **(page 26, lines 25-27)**; and

applying the test signals **(page 8, lines 24-26)** through the electrical connectors **(page 23, line 34 to page 24, line 3)**, through the suspended plate **(page 23, lines 24-30)**, and through the substrate to the wafer **(page 8, lines 25-26)**.

In addition to the amendments to claims 77-82, claims 91-96 have been added. Added independent claim 91 is similar to claim 77. A reading of claim 91 on the specification and drawings is as follows.

91. In a test system **(82-Figure 8, page 26, line 9 to page 27, line 2)** including a testing apparatus **(78-Figure 8, page 26, lines 10-21)** for a semiconductor wafer **(12-Figure 1)**, a method **(page 8, lines 13-26)** for testing the wafer comprising:

suspending **(antecedent basis for "suspending" on page 21, line 3)** a substrate **(16-Figure 7B, page 23, lines 20-24)** on the testing apparatus;

providing a force applying mechanism **(32-Figure 1 page 12, lines 19-21)** on the testing apparatus comprising a plurality of electrical connectors **(42-Figure 7B, antecedent basis for "electrical connectors" on page 14, lines 18-19)** configured to bias the substrate against the wafer;

biasing the substrate against the wafer using the force applying mechanism **(page 26, lines 25-27)**; and

applying test signals **(page 8, lines 24-26)** through the electrical connectors **(page 23, line 34 to page 24, line 3)** and the substrate to the wafer **(page 8, lines 25-26)**.

Rejections Under 35 USC §102(e)

Claims 77-82 have been rejected under 35 USC §102(e) as being anticipated by Nakata et al. (US Patent No. 6,005,401). Amended claims 77-82, and added claims 91-96, include recitations which make the claimed method both novel and unobvious over Nakata et al.

In this regard, independent claim 77 includes the step of "providing...a suspended plate, a substrate on the suspended plate, and a force applying mechanism comprising a plurality of electrical connectors in contact with the suspended plate in electrical communication with the test circuitry". Nakata et al. does not disclose or suggest the step of providing a suspended plate and a force applying mechanism comprising electrical connectors.

In addition, independent claim 77 recites the step of "biasing the substrate against the wafer using the suspended plate and the force applying mechanism". Nakata et al. does not disclose or suggest a biasing step using a suspended plate and electrical connectors.

Further, independent claim 77 recites the step of "applying the test signals through the electrical connectors, through the suspended plate and through the substrate to the wafer." Nakata et al. does not disclose or suggest an applying step using a suspended plate, and electrical connectors configured to apply a biasing force to the suspended plate.

Added independent claim 91 includes the step of "suspending a substrate on the testing apparatus". Nakata et al. does not disclose or suggest such a suspending step.

In addition, added independent claim 91 recites the step of "providing a force applying mechanism comprising electrical connectors". Further, independent claim 91 recites the step of "applying test signals through the electrical connectors and the substrate to the wafer". Nakata et al. does not disclose or suggest an applying step using a suspended substrate and electrical connectors configured to apply a biasing force to the suspended substrate.

Conclusion

In addition to the claim amendments, the specification has been amended to correct informalities on pages 13 and 19 (46A changed to 46B).

Favorable consideration and allowance of amended claims 77-82 and added claims 91-96 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

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Respectfully submitted:

STEPHEN A. GRATTON
Registration No. 28,418
Attorney for Applicants

2764 S. Braun Way
Lakewood, CO 80228
Telephone: (303) 989-6353
FAX (303) 989-6538

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August 28, 2003
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Stephen A. Gratton, Attorney for Applicants